Ka-BAND 2-WATT POWER GaAs MMIC

Shigemitsu Arai, Tomohiro Yoshida, Kenichiro Kai,
Shinji Takatsuka, Yuji Oda and Shigeru Yanagawa

Microwave Solid-State Department
Komukai Works, Toshiba Corporation
1, Komukai-Toshiba-cho Saiwaiku Kawasaki, 210, Japan

ABSTRACT

High-power Ka-band power GaAs MMICs have been developed using distributed-element impedance transforming technique. At 30 GHz, an output power of 2 W with 3.3 dB gain and a saturation output power of 3 W have been obtained from 9.6 mm gate width power GaAs FET MMIC. These output powers are the highest values reported to date on Ka-band FETs.

INTRODUCTION

Ka-band High-power and high-gain GaAs FETs are required in various systems such as satellite communications and electronic warfare systems. Oda et al. have reported a power GaAs MMIC providing an output power of 1.6 W with 3.0 dB gain, using Be co-implantation technique [1]. In order to get higher power, total gate width of device must be made larger while lateral chip dimensions must be made smaller than the wavelength to avoid gain degradation due to out-of-phase operation [2].

The purpose of this paper is to report on high-power Ka-band GaAs FET MMIC with on-chip matching circuit comprising power divider and combiner. At 30 GHz, the developed MMIC with 9.6 mm total gate width yeilds an output power of 2 W with 3.3 dB gain, 11 % power-added efficiency and 3 W saturation output power. The output powers are the highest value reported to date on single-chip Ka-band power GaAs FETs.

WAFER PROCESSING

The starting wafers were undoped LEC semi-insulating GaAs substrates with 2 inch diameter and (100) orientation. The active layers were formed using Be co-imlantation technique [1]. Si was implanted twice with doses of 7.0 E12 cm^{-2} and 2.0 E12 cm^{-2} at energies of 150 keV and 50 keV, respectively. After Si implantation, Be implantation was performed with a dose of 6.0 E11 cm^{-2} at 130 keV to make a steep carrier profile in the active layer. The peak carrier concentration and the depth of the active layer were around 2.7 E17 cm^{-3} and 0.13 μm, respectively. The source and drain electrodes were formed by alloying Pt/AuGe. Aluminum was used for the gate electrode. The gate length was 0.5 μm. Air bridges and via holes were used to reduce parasitic capacitance and inductance, respectively. The GaAs substrate was thinned down to about 30 μm, and a gold PHS (plated heat sink) with 50 μm thickness was formed on the backside of the substrate.

DEVICE DESIGN

A total gate width of 9.6 mm was chosen for the 2 W GaAs FET MMIC. The gate-to-gate spacing was selected to be 14 μm, taking thermal resistance and device processing into account.

As mentioned previously, the lateral dimension of FET chip should be as small as possible for in-phase operation. From this point of view, a longer gate finger is preferable, except for a sacrifice of gain. To decide the gate finger length, rf performance comparison was made between FETs with different gate finger lengths. Fig.1 shows output power and power-added efficiency vs.

CH2725-0/89/0000-1105$01.00 © 1989 IEEE

input power characteristics of FETs with gate finger lengths of 50 μm and 80 μm at drain-source voltage (Vds) of 7 V. The total gate width of the FETs is 4.8 mm. The 50 μm and 80 μm FETs deliver output powers (at 1dB gain comression point) of 32.7 dBm and 32.8 dBm with gains of 3.2 dB and 3.4 dB, and power-added efficiencies of 16.5 % and 17.5 % at 30 GHz. Since no difference has been seen in the output power performance, the gate finger length of 80 μm has been chosen for the 2 W power GaAs MMIC.

Fig.2 shows the equivalent circuit of the developed 2 W power GaAs MMIC with a total gate width of 9.6 mm. The MMIC consists of four FET cells, each comprising five unit FETs. The matching circuitries consist of transmission lines with various line widths, transforming low FET impedance into high one and working as power divider and combiner. The matching circuit was optimized using computer. The minimum transmission line width has been determined to be 50 μm from a circuit loss consideration.

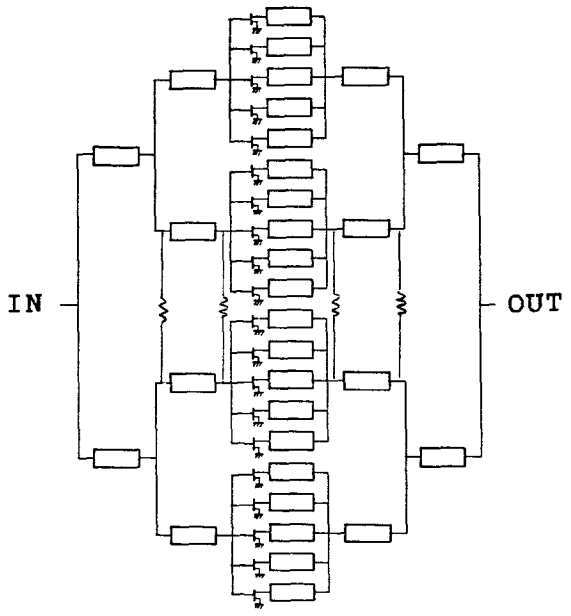

Fig.2 Equivalent circuit of developed 2 W GaAs MMICs.

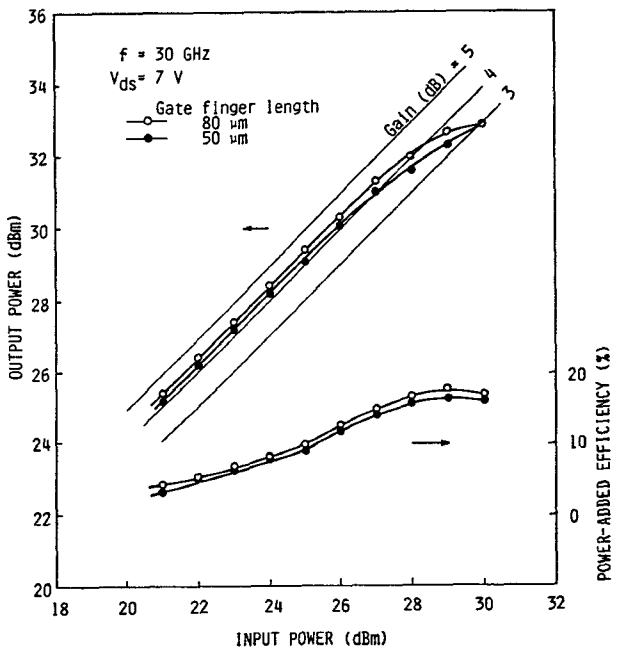

Fig.1 Output power and power-added efficiency vs. input power at 30GHz of 4.8 mm width MMICs with gate finger length of 50 μm and 80 μm.

Fig.3 shows the top view of the 9.6 mm width MMIC chip. The chip size is 2.4 mm x 3.1 mm. It is to be noted that the lateral chip length of 2.4 mm is nearly the same as that of 4.8mm width 1 W GaAs MMIC reported in [1]. The present chip contains oscillation damping resistors to realize stable operation.

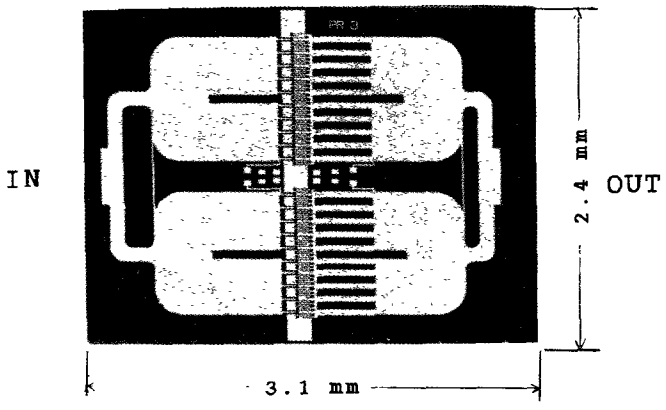

Fig.3 Top view of 2 W MMICs with gate width of 9.6 mm.

DC AND RF PERFORMANCE

MMICs were dc screened before assembling on a chip carrier. Typical drain saturation current, pinch off voltage and transconductance are 3.0 A (310 mA / mm), -3.5 V and 1160 mS (120 mS/ mm), respectively for the 9.6 mm width FET. The gate-drain breakdown voltage is typically 14 V at a reverse current of 400 μA.

Fig.4 shows output power and power-added efficiency vs. input power characteristics of the 9.6 mm width MMIC in comparison with those of the 4.8 mm and the 2.4 mm width MMICs. At 30 GHz, a power gain of 3.3 dB at 2 W output power, a 1-dB gain compression output power of 2.6 W with 2.7 dB gain and a saturation output power of 3.0 W with 2.0 dB gain have been obtained with the 9.6 mm width MMIC. The 4.8 mm and 2.4 mm width MMICs deliver 1-dB gain compression output powers of 1.9 W with 3.4 dB gain and 0.7 W with 4.2 dB gain and saturation output powers of 2.4 and 1.1 W both with 2 dB gain, respectively. The maximum power-added efficiencies are 12.0 %, 17.7 % and 19.6 % for the 9.6 mm, 4.8 mm and 2.4 mm width MMICs, respectively.

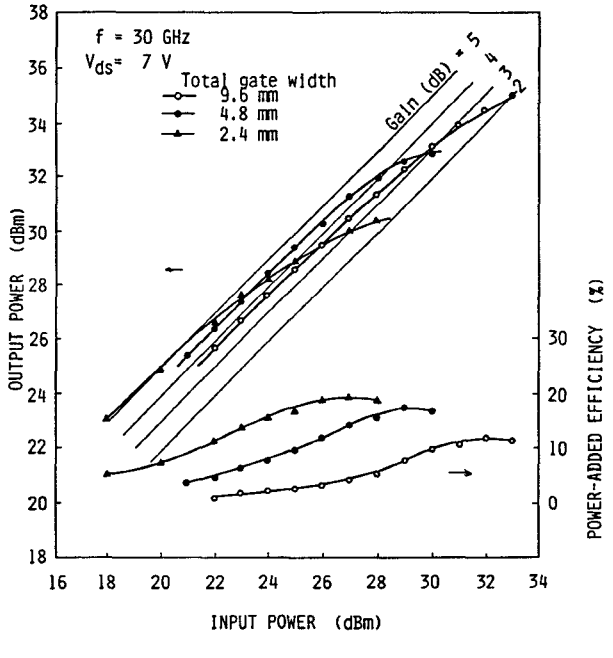

Fig.4 Output power and power-added efficiency vs. input power at 30 GHz for 2.4 mm, 4.8 mm and 9.6 mm width MMICs.

Fig.5 shows saturation output power, linear gain and maximum power-added efficiency vs. total gate width at 30 GHz. It can be seen that the power combining efficiencies of 4.8 mm and 9.6 mm width MMICs are 80 % [1] and 64 %, respectively, with reference to 2.4 mm width unit FET cell.

Fig.6 shows a typical frequency response of output power of the 9.6 mm width MMIC. More than 2 W of output power has been obtained over the frequency range of 29.5-30.3 GHz at an input power of 1 W.

The thermal characteristics of MMICs have been measured by using an infrared scanning microscope. Fig.7 shows a measured typical temperature profile of the 9.6 mm width MMIC baised at Vds= 7 V and Ids= 1.4 A, indicating a uniform thermal operation of each unit FET. The thermal resistance evaluated from the peak temperature of active area (138 °C) is about 3.5 °C/W. From this, the channel temperature increase is estimated to be about 50 °C at 2 W output power operation, which guarantees a reliable high-power operation.

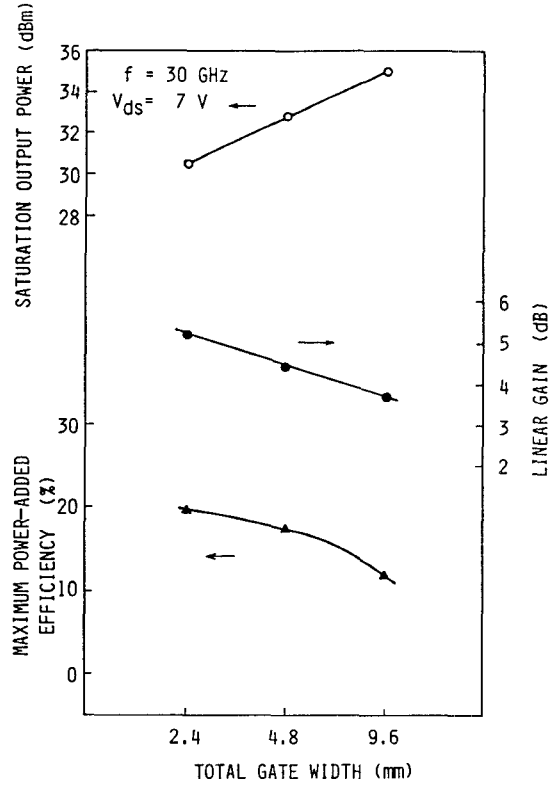

Fig.5 Saturation output power, linear gain and maximum power-added efficiency vs. total gate width at 30GHz.

CONCLUSION

High-power Ka-band power GaAs MMICs have been developed using distributed-element impedance transforming technique. The MMIC with 9.6 mm gate width FET delivered a CW output power of 2 W with 3.3 dB gain and a saturation output power of 3 W. It is expected that those MMICs will greatly contribute to improving the output power of Ka-band soloid-state power amplifiers. Improvements for high-gain performance can be achieved through reduction of gate length and gate resistance.

ACKNOWLEDGMENT

The authors wish to thank M. Kuroda for his encouragement and helpful discussions and Dr. M. Ohtomo for critical reading of the manuscript.

REFERENCES

[1].Y.Oda et al. Ka Band 1 WATT GaAs MMICs",IEEE MTT-S International Microwave Symposium Digest, June 1988,pp413-416.

[2].G.C.Taylor et al. High-Efficiency 35-GHz GaAs MESFET's", IEEE Trans. Electron Devices, vol.ED-34,pp. 1259-1262, June 1987.

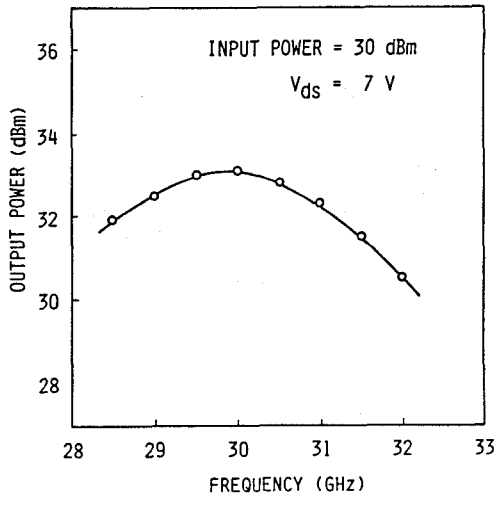

Fig.6 Output power vs. frequency of 9.6 mm width MMICs.

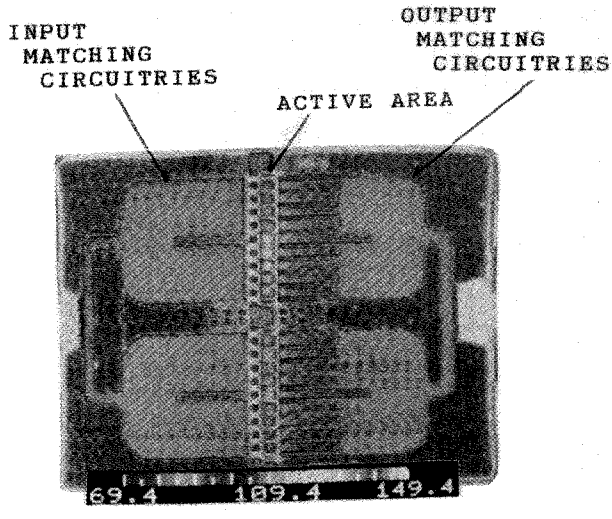

Fig.7 Typical temperature profile of 9.6 mm width MMICs.